WS2814

Single-line 256-level grayscale four-channel dual-input constant current LED driver IC

Main feature

- The R, G, B, and W output ports can withstand 20V, and the DIN1 and DIN2 ports can withstand 9V.
- The chip has a built-in voltage regulator. For power supplies of 24V and below, only a resistor needs to be connected to the IC VDD pin, and no external voltage regulator is required.
- Built-in signal shaping circuit. After any pixel receives the signal, it undergoes waveform shaping before outputting it, ensuring that line waveform distortion will not accumulate.
- Built-in power-on reset and power-off reset circuits.
- The PWM control end can achieve 256-level adjustment, with a scanning frequency of 2KHz.
- Serial cascade interface, which can complete data reception and decoding through a signal line.
- Breakpoint resume transmission, in the event of a single chip being damaged, does not affect the overall display effect.
- No circuit needs to be added when the transmission distance between any two points does not exceed 2 meters.
- The color of the light is highly consistent, and the cost-effectiveness is high.
- When the refresh rate is 30 frames/second, the number of cascades is not less than 1024 points.
- The data transmission speed can reach 800Kbps.

Main application areas

- LED full-color luminous character light string, LED full-color soft light bar, hard light bar, LED guardrail tube.
- LED point light source, LED pixel screen, LED special-shaped screen.

Product Overview

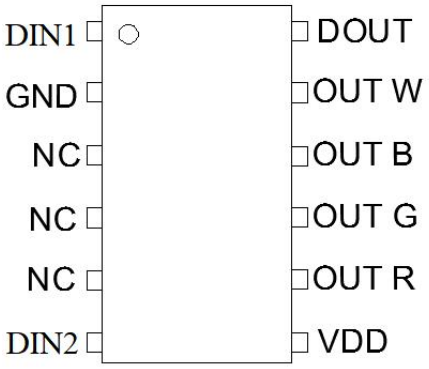
WS2814 is a four-channel LED drive control dedicated circuit. The chip contains an intelligent digital interface data latch signal shaping and amplification drive circuit, a high-precision internal oscillator, a 20V high-voltage programmable constant current output driver, and a high-precision constant current control module, which effectively ensures that the color of the pixel light on the drive circuit is highly consistent.

The data protocol uses a single-line return-to-zero code communication method. After the chip is powered on and reset, the DIN1 end receives the data transmitted from the controller. The first 32-bit data sent is extracted by the first chip and sent to the data latch inside the chip. The remaining data is shaped and amplified by the internal shaping processing circuit and then forwarded to the next cascaded pixel through the DO port. After each pixel is transmitted, the signal is reduced by 32 bits. The chip uses automatic shaping and forwarding technology, so that the number of cascaded pixels is not limited by signal transmission, but only by the signal transmission speed requirements.

The data latch inside the chip generates different duty cycle control signals at the OUTR, OUTG, and OUTB control terminals according to the received 32-bit data. When waiting for the RESET signal to be input at the DIN1 terminal, all chips will synchronously send the received data to each segment. The chip will receive new data again after the signal ends. After receiving the initial 32-bit data, the data port is forwarded through the DO port. Before the chip receives the RESET code, the original outputs of the OUTR, OUTG, and OUTB pins remain unchanged. After receiving a low-level RESET code of more than 280μs, the chip will output the 32-bit PWM data pulse width just received to the OUTR, OUTG, and OUTB pins.

Available in SOP14 package.

Pin Configuration



Pin function

Pin number	Pin Symbols	Pin name	Function description
1	DIN1	Data 1 Input	Display data 1 input
2	GND	Ground	Signal ground and power ground
3/4/5	NC	Null pin	-
6	DIN2	Auxiliary data input	Display data 2 input
7	VDD	Logic Power Supply	IC Power Supply
8	OUTR	LED driver output	RED (red) PWM control output
9	OUTG	LED driver output	GREEN PWM control output
10	OUTB	LED driver output	BLUE (blue) PWM control output
11	OUTW	LED driver output	WHITE (white) PWM control output
12	DOUT	Data output	Display data cascade output

Maximum rating（Unless otherwise specified，T_A=25℃，V_{SS}=0V）

Parameter	Symbol	Range	Unit
Logic supply voltage	V_{DD}	+3.7~+5.3	V
Logic input voltage	V_I	-0.7～VDD+0.7	V
R, G, B output port withstand voltage	Vout	20	V
Operating temperature	Topt	-25～+85	℃
Storage temperature	Tstg	-40~+150	℃

Electrical parameters（Unless otherwise specified，TA=-20～+70℃，VDD=4.5～5.5V，VSS=0V）

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Test Conditions
R, G, B low level output current	I_{OL}	15.5	16.5	17.5	mA	
Low level output current	I_{dout}	10	——	——	mA	Vo=0.4V，D_{OUT}
Signal input current	I_I	——	——	±1	μA	$V_I=V_{DD}/V_{SS}$
High level input	V_{IH}	$0.7V_{DD}$	——	VDD+0.7	V	D_{IN}
Low level input	V_{IL}	-0.7	——	$0.3\ V_{DD}$	V	D_{IN}
Hysteresis voltage	V_H	——	0.35	——	V	D_{IN}

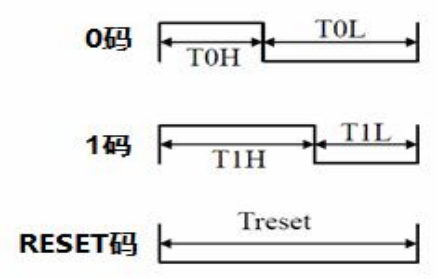
Switching characteristics（Unless otherwise specified，TA=-20～+70℃，VDD=4.5～5.5V，VSS=0V）

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Test Conditions
Transmission delay time	tPLZ	——	——	300	ns	CL=15pF, DIN→DOUT, RL=10KΩ
Fall time	tTHZ	——	——	120	μs	CL=300pF, OUTR/OUTG/OUTB/OUTW
Fall time Data transfer rate	*FMAX*	600	——	——	Kbps	Duty cycle 50%
Input capacitance	CI	——	——	15	pF	——

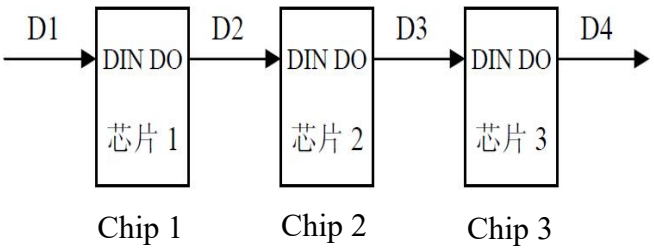
Data transmission time

T0H	0 code，High level time	220ns~380ns
T1H	1 code，High level time	580ns~1μs
T0L	0 code，Low level time	580ns~1μs
T1L	1 code，Low level time	580ns~1μs
RES	Frame unit, low level time	280μs or more
Data cycle	T1H+T1L、T0H+T0L≥1.25us	

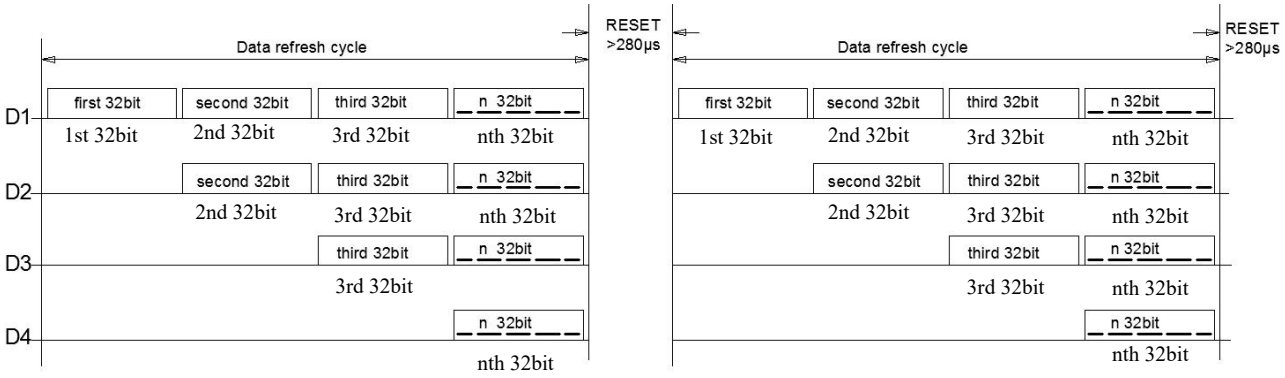
Timing waveform
Input code type:



Connection method:

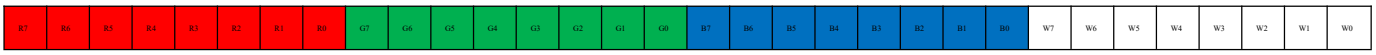


Data transmission method



Note: D1 is the data sent by the MCU, and D2, D3, and D4 are the data automatically shaped and forwarded by the cascade circuit.

32-bit data structure

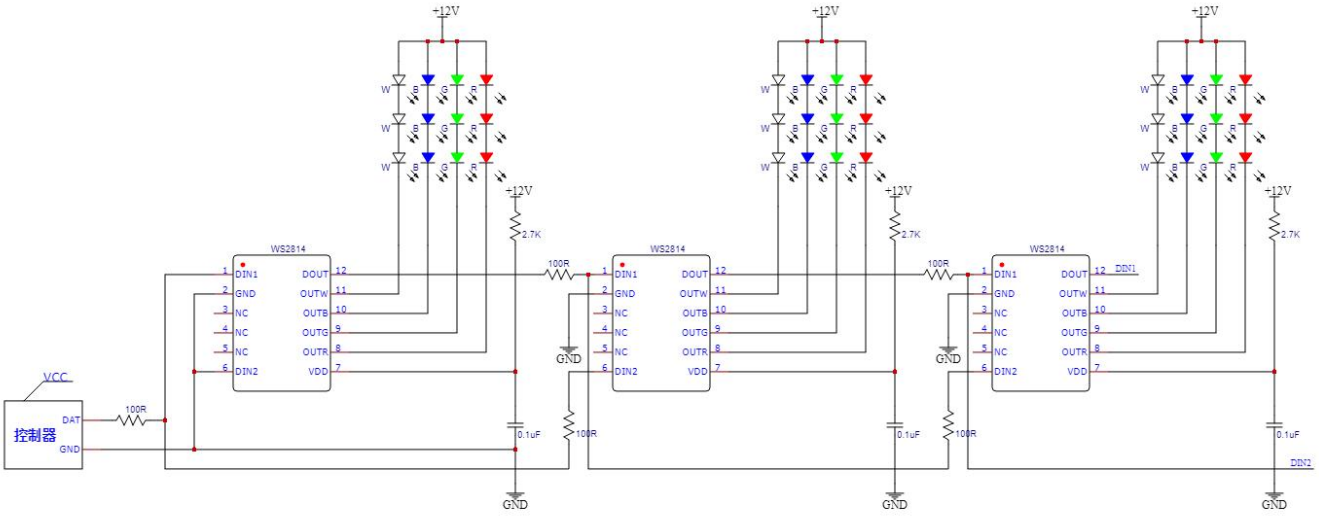


Note: The high bit is sent first, and the data is sent in the order of RGBW.

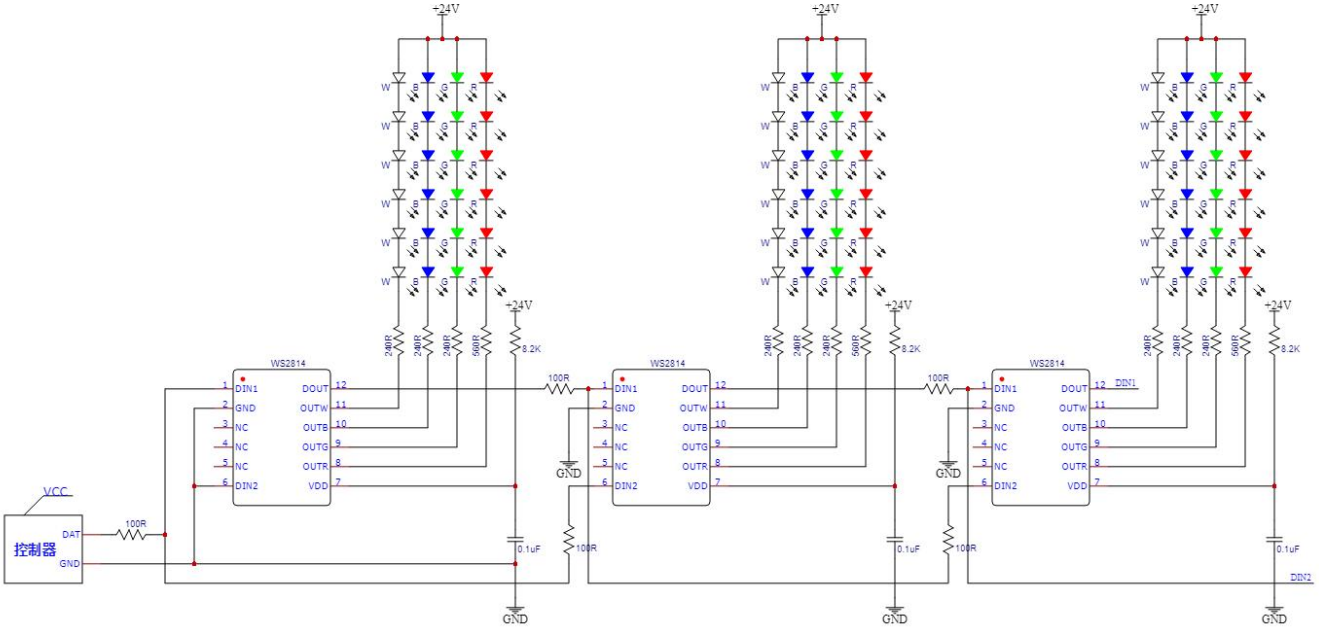
Typical application circuit

12V power supply application reference circuit (each channel with 3 LEDs):

12V供电应用参考电路（每通道带3颗LED）：

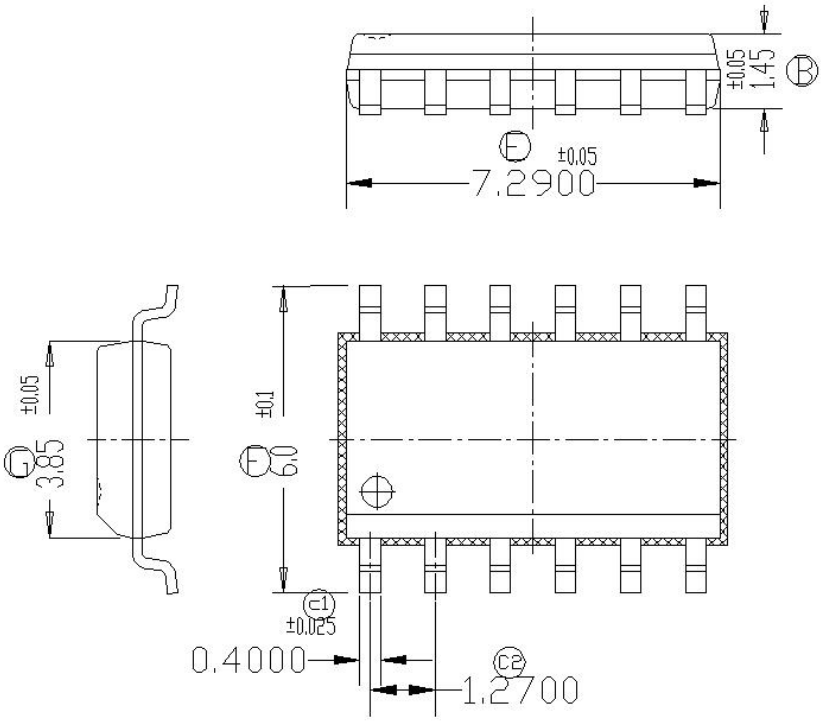


24V供电应用参考电路（每通道带6颗LED）：24V power supply application reference circuit (each channel with 6 LEDs):



Package diagram and parameters

- **SOP12 package 4K/roll**



Symbol	Dime nsions In Millimeters		
	Min.	NOM.	Max.
B	1.400	1.450	1.500
E	7.240	7.290	7.340
F	5.900	6.000	6.100
G	3.800	3.850	3.900
c1	0.375	0.400	0.425
c2	-	1.270	-

File Change Log

Version number	Status	Summary of changes	Revision date	Revised by	Approver
V1.0	N	New	20190410	Dong Le	Shen Jinguo
V1.1	M	Modify	20190522	Dong Le	Shen Jinguo
V1.2	M	Modify	20210401	Dong Le	Yin Huaping
V1.3	M	Add typical application circuit	20211125	Xie Yanfan	Yu Xinghui
V1.4	M	Detail parameter modification	20220726	Hu Jin	Yu Xinghui

Note: The initial version number is V1.0; after each revision is approved, the version number is incremented by "0.1";
Status includes: N--New, A--Add, M--Modify, D--Delete.