

# **Characteristic Description**

TM512BCE is a DMX512 differential parallel protocol LED driver chip with 16-bit gray scale and enhanced gamma correction 2.2, which is more suitable for human visual perception.3 channel with high precision and constant output. TM512BCE decoding technology accurately decodes DMX512 signals, which can be compatible with and expand DMX512 protocol signals. TM512BCE completely adaptively decodes DMX512 signals with transmission frequency within 200 kbps ~ 1000 kbps, without setting the rate, and can address up to 4096 channels. TM512BCE has built-in E2PROM, which needs no external connection and supports online code writing. the chip provides three high-precision constant output channels with withstand voltage of 30V up to 80ma, and the output size of electricity is set by an external resistor. . High port refresh rate greatly improves picture refresh. TM512BCE can short-circuit multiple sets of constant output interfaces to expand current drive capability. It is mainly designed for LED lighting system of building decoration and stage lighting effect. The abnormality of one chip does not affect the normal work of other chips at all, and the maintenance is simple and convenient. This product has excellent performance and reliable quality.

# **Functional Characteristics**

- Compatible and extended DMX512(1990) signal protocol
- > Control mode: differential parallel connection, maximum support for 4096 channel addressing
- High-speed DMX512 supplements the patent of algorithm, which can completely adaptively decode DMX512 signals with transmission rate of 200 kbps ~ 1000 kbps
- The built-in 485 module has the advantages of high differential signal resolution and large differential input impedance, which can greatly enhance the load-carrying capacity
- Built-in E2PROM, no external E2PROM is needed
- AB line writes code online, which can write code automatically at one time, and supports the mode of writing code after installation first
- > E2 address code double backup mode, partial E2 damage does not affect address code reading
- The output port has 16-bit gray scale control and adopts gamma correction 2.2 enhancement, which is more suitable for human visual perception
- Screen refresh up to 2KHz
- Built-in 5V voltage regulator
- > OUTR/OUTG/OUTB output withstand voltage is greater than 30V
- > OUTR/OUTG/OUTB four-bit constant output channel
- External output constant current adjustable resistor, the current range of each channel is 3 ~ 80mA
- A fixed 18mA constant current output is built into SSOP10 package
- > ±3% inter-channel electrical difference value, ±5% inter-chip electrical difference value
- Power-on self-test lights up in blue. After code writing is successful, the first address lights up in red, and other addresses lights up in white for breakpoint identification.
- > The new address does not need to be re-powered when it takes effect
- > 80 ns output channel hysteresis reduces surge current interference
- Industrial grade design, stable performance
- Package form: SSOP10

# **Application Field**

Point light source, line lamp, wall washing lamp, stage lighting system, indoor and outdoor video wall, decorative lighting system



Internal structure block diagram

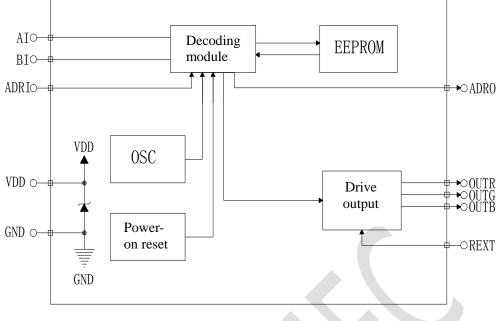
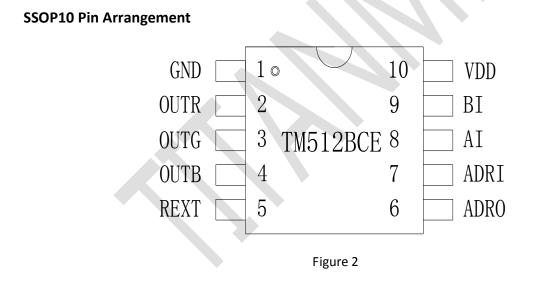


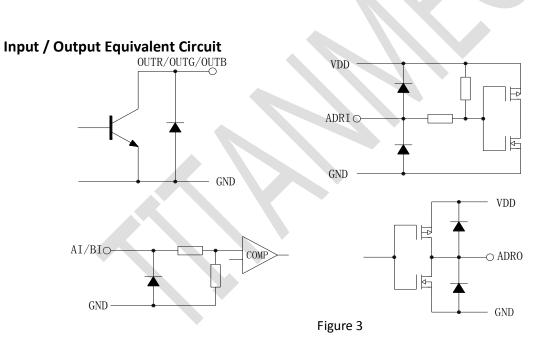
Figure 1





SSOP10 pin function

Pin name	Pin serial number	I/O	Function description
GND	1		Negative power supply
OUTR/OUTG/OUTB	2~4	0	PWM output port, fixed 18mA constant current output.
REXT	5	I	A constant current feedback end for adjusting the output current to the ground resistance
ADRO	6	О	Address writing code line output
ADRI	7	I	Address writing code line input, built-in pull-up
AI	8	I	Differential signal, positive, built-in pull-up.
BI	9	I	Differential signal, negative, built-in pull-down.
VDD	10		Power cathode





Integrated circuit is an electrostatic sensitive device, which is easy to generate a large amount of static electricity when used in dry season or dry environment. Electrostatic discharge may damage the integrated circuit. Tianwei Microelectronics recommends taking all appropriate integrated circuit preventive measures. Improper operation and welding may cause ESD damage or performance degradation, and the chip cannot work normally.



# **Working Conditions**

## 1. Ultimate Working Conditions

Tested at 25 $^\circ C$ , VDD=5V, unle	ess otherwise specified	TM512BCE	11	
Parameter name	Parameter symbol	limit value	Unit	
Logic supply voltage	Vdd	+5.5~+6.5	V	
Output port withstand voltage	Vout	30	V	
Logic input voltage	Vi	-0.5~Vdd+0.5	V	
Working temperature	Topt	-45~+85	°C	
Storage temperature	Tstg	-55~+150	°C	
Antistatic	ESD	4000	V	
Package power consumption	Pd	400	mW	

(1) Long-term operation of the chip under the above-mentioned limit parameters may cause the reliability of the device to be lowered or permanently damaged. Tianwei Microelectronics does not recommend that any parameter reach or exceed these limit values in actual use.

(2) All voltage values are tested against the system ground.

#### 2. Recommended Working Conditions

Unless otherwise s -40°C~+65°C.	pecified, VDD=	5V when tested at	TM512BCE		11	
Parameter name	Parameter symbol	Test condition	Minimum value	Typical value	Maximu m value	Unit
Logic supply voltage	Vdd		2.6	5.5	6	V
High level input voltage	Vih	-	0.7Vdd		Vdd	V
Low level input voltage	Vil	-	0	_	0.3Vdd	V
Output port withstand voltage	Vout				30	V

#### **Chip Parameters**

#### 1. Electrical specification

Unless otherwise specified, tested at -40 $^{\circ}C$ +65 $^{\circ}C$ , VDD = 4.5 V ~ 5.5V, GND=0V.						
Parameter name	Parameter symbol	Test condition	Minimum value	Typical value	Maximum value	Unit
Low level output current	lol	Vo=0.4V, ADRO	10	-	-	mA
High level output current	loh	Vo=4.0V, ADRO	10	-	-	mA
Differential input common mode voltage	Vcm				8	v
Differential input current	lab	VDD=5V			28	μA
Differential input threshold voltage	Vth	0V <vcm<8v< td=""><td>-0.2</td><td></td><td>0.2</td><td>v</td></vcm<8v<>	-0.2		0.2	v
Differential input hysteresis voltage		Vcm=0V		70		mV
Differential input	Rin			280		KΩ



impedance						
Output pin current	lsink	OUTR, OUTG, OUTB (REXT resistance to ground )	3		80	mA
High level input voltage	Vih	ADRI	0.7Vdd	-		v
Low level input voltage	Vil	ADRI	-	-	0.3Vdd	v
Current offset (inter-channel)	dlout	Vds=1V,Iout=17mA		±1.5	±3.0	%
Current offset (between chips)	dlout	Vds=1V,Iout=17mA		±3.0	±5.0	%
Voltage offset VS-Vds	%dVds	1V <vds<3v< td=""><td></td><td>±0.1</td><td>±0.5</td><td>%/V</td></vds<3v<>		±0.1	±0.5	%/V
Voltage offset VS-Vdd	%dVds	4.5V <vdd<5.5v< td=""><td></td><td>±1.0</td><td>±2.0</td><td>%/V</td></vdd<5.5v<>		±1.0	±2.0	%/V
Dynamic current loss	IDDdyn	VDD=5V	Non-loaded		4	mA
Consumed power	PD	Ta=25 ℃	-	-	250	mW

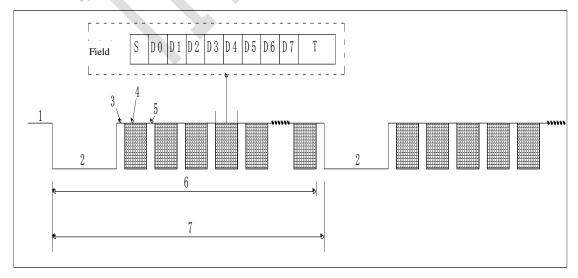
## 2. Switching Characteristics

Unless otherwise specified, tested at $-40^{\circ}C^{+65}C$ , VDD = 4.5V ~ 5.5V, GND=0V.		TM512BCE			Unit	
Parameter name	Parameter symbol	Test condition	Minimum value	Typical value	Maximu m value	Onit
Transmission delay time	Tflz	C1=15pF,Din→Dout,R1=10KΩ	-	-	300	ns
Falling time	Tthz	C1=300pF,OUTR/OUTG/OUTB		-	120	us
Data transmission rate	F	-	-	500	1000	Kbps
Input capacitance	Ci		-	-	15	рF

## **Function Description**

## 1. Communication Data Protocol:

TM512BCE data reception is compatible with standard DMX512 (1990) protocol and extended DMX512 protocol, and the transmission rate is 200kbps~1000kbps adaptive decoding. The protocol waveform is as follows: the chip is input differentially by AI and BI, and the time sequence waveform of AI is shown in the figure, and BI is opposite to AI.





Grade	Describe	Minimum value	Typical value	Maximum value	Unit
	Bit rate	200	500	1000	Kbps
	Bit time	1	2	5	μs
S	Start bit	1	2	5	μs
D0 <b>~</b> D7	8-bit data	1	2	5	μs
Т	2-bit stop bit	2	4	10	μs
1	Mark before reset	0		1000000	μs
2	reset signal	88		1000000	μs
3	Mark after reset	8		1000000	μs
4	Field (note1)	11	22	55	μs
5	Account for between fields	0		1000000	μs
6	Length of packet	1024		1000000	μs
7	Reset signal interval	4096		1000000	μs

Note1: The field consists of 11 bits, including 0 start bit, 8 data bits and 2 stop bits. Where the start bit of 0 is low level, the stop bit is high level and the data in the data bit is 0, then the corresponding time period is low level; if the data is 1, the corresponding time period is high. 0 The bit length of the start bit stop bit and the data bit must be the same.

#### 2. IC Receiving Instructions:

1. When reset signals appear on AI and BI lines, IC enters the receiving ready state. The address counter is cleared.

2. The first field in the data packet is the starting field, and its 8-bit data must be "0000\_0000", which is not used as display data. The valid fields for display start from the second field, and the second field of DMX512 data packet is the first field of valid data. The adaptive data transmission rate of IC is 200 kbps ~ 1000 kbps. The field durations corresponding to different rates are different, but no matter the transmission frequency is 200Kbps/500Kbps/1000Kbps, it is only necessary to ensure that the duration of all valid fields is the same as that of the starting field.

3. When IC receives data, the interval between two reset signals cannot be less than 4ms, and the frame frequency cannot be greater than 250Hz even if the number of parallel connection points is very small.

#### 3. Precautions for the Controller to Send Data:

1. For the standard DMX512(1990) protocol, if a sub-port of the controller is connected to 512 channels, that is, 170 pixels, and the refresh rate is 30Hz, then the time width of each frame is 33.33ms, the time for transmitting 1bit is  $4\mu$ s, and the effective data time width is  $88+4\mu$ s\*11bit\*512=22.7ms, then each frame During this time interval, the data line remains high until the next reset signal.

2. TM512BCE requires that the reset signal interval of each data packet of the controller should not be less than 4ms, that is, the highest frame frequency should not be higher than 250Hz, otherwise the picture may not be displayed normally.

#### 4. Matters Needing Attention in Writing Code:

1. After the code writing is completed, the IC driving red light of the first address code is always on, and the other address IC driving white lights are always on. The newly written address code takes effect and can be used as breakpoint discrimination.

2. Don't take down the AB line after writing code, and test it with the special test program of the code writer to confirm whether the code is completely correct.

3. The address input terminal lines on the AI and BI ports of the code writer should be pulled out from the code writer after the code writing is completed, so as to avoid wrong code writing when the code writer is out of order. After the code writing line is pulled out, it can be hung up and wrapped with insulating tape without special grounding.

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## 5. Differential Bus Connection Considerations:

1. There must be common ground between controller and IC, and between IC and IC, so as to prevent excessive common-mode voltage from penetrating IC. Multiple IC nodes can be reliably connected by using shielding layer as common ground wire, which can be reliably grounded at one point, but cannot be grounded at two ends or multiple ends.

2. The protection resistors connected in series between AI line and BI line on the board and IC shall be consistent, and the routing mode of AIBI line on the board from pad to IC shall be consistent as far as possible.

3. As far as possible, AI and BI buses shall adopt shielded twisted pair (especially in the common project of high-current and weak-current wiring troughs, near the transmission tower or in areas with more lightning) to reduce interference and lightning impact. Ordinary super-category 5 shielded twisted pair can be used, but pay attention to the purchase of copper wire.

4. In 485 bus, the distance between node 485 and trunk should be minimized. It is generally recommended that 485 bus adopt hand-in-hand bus topology. The star structure will produce reflected signals, which will affect the communication quality of 485. If the distance between node 485 and the trunk of 485 bus must exceed 1m during construction, it is recommended to use 485 repeater to make a bifurcation of 485 bus. If star topology is required during construction, 485 hub should be used.

5. With the extension of transmission distance, 485 bus will produce echo reflection signal. If the transmission distance of 485 bus is long, it is suggested to connect a 120 ohm terminal matching resistor in parallel with AI and BI lines at the end of 485 communication during construction.

## 6. Enhanced Gamma Correction 2.2 Description:

1. TM512BCE has its own gamma correction with a coefficient of 2.2, which corrects 256 gray levels to 65536 gray levels.

2. TM512BCE adopts enhanced design mode, and the turn-on time of RGB output is: basic turn-on time+gray time after correction. That is to say, a basic turn-on time is added on the basis of each gray-scale time, which aims to compensate the actual turn-on delay and the large difference of turn-on time of different high-power constant-current driving ICs in high-power applications, so as to ensure that the first-level gray-scale can be obviously felt by human eyes when matched with different high-power constant-current ICs in most cases.

3. Positive polarity: the basic opening time is about 85ns.

# **Constant Current Module**

# 1. Output Constant Current Setting:

OUTR, OUTG, OUTB are constant current outputs, and the maximum current can reach 80mA. It is not recommended to set the current to a larger value. The value of constant current is determined by the resistance of REXT to ground. the constant current of SSOP10 package is fixed at 18mA, and the current formula is:

lout=48/(400+Rext) (1)

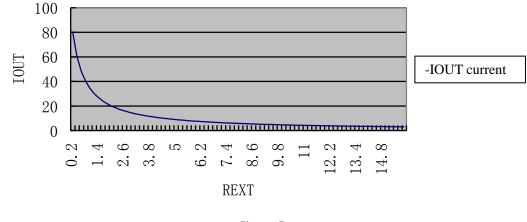
Rext=(48/lout)-400 (2)

REXT is the resistance connected between Rext pin and ground, in  $\omega$ , and  $\Omega$ ,lout is the current output by OUTR, OUTG, OUTB ports.

Current value (mA)	Rext resistance (Ω)
18	2266.67
20	2000
36	933.33
60	400

The relationship between IOUT current and REXT







## 2. Constant Current Curve:

TM512BCE has excellent constant current characteristics, and the current difference between channels and even between chips is extremely small.

(1) The current error between channels is  $\pm 3\%$ , while the current error between chips is  $\pm 3\%$ .

(2) When the load terminal voltage changes, the output current of TM512BCE is not affected, as shown in the following figure.

(3) According to the curve relationship between the current I of TM512BCE output port and the voltage Vds applied to the port in the following figure, the smaller the current I is, the smaller the Vds required in constant current state is.

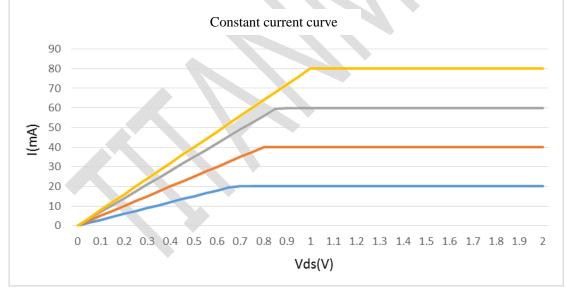


Figure 6



# **Application Information**

## 1. Application Figure : RGB 3-color application

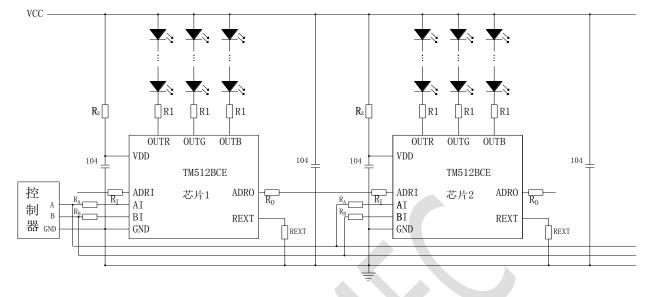


Figure 7

Note: 1.A and B lines are used to write codes. When writing codes, the code writer or controller does not need to be connected with the ADRI of the first IC.

2.Pay attention to the selection of voltage dividing resistor R1 to avoid excessive power consumption of IC.

3. The REXT port must add a resistor to the ground to set the output current, and this port cannot be left floating.

4. The 104 capacitance of VCC to ground is the recommended value when the channel current is set to 20mA. If the channel current is larger, the capacitance value should be increased. For example, if the channel current is set to 40mA, the capacitance value above 105 is recommended.

	24V	12V	5V
$R_{Z(\Omega)}$	2K~2.4K	750~820	82
$R_{I(\Omega)}$	300~500	300~500	300~500
$R_{O(\Omega)}$	300~500	300~500	300~500
$R_{A(\Omega)}$	3K~5K	3K~5K	3K~5K
$R_{B(\Omega)}$	3K~5K	3K~5K	3K~5K

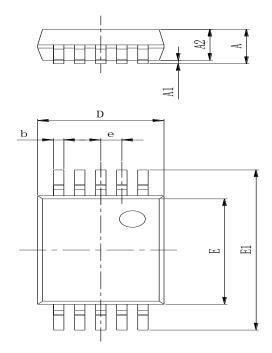
#### 2. Component selection table

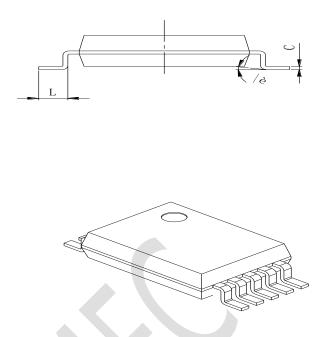
#### (1) Selection of the value of lamp string resistance R

As the long-term power consumption of the package is not recommended to be greater than 400mW, the IC power consumption should be set to be less than 400mW. With the increase of the driving current, the output voltage Vout of the chip channel should be reduced, that is: With 400mW > 5.2V\*10mA + Vout \* lout \* N(N is the number of channels, Vout is the channel port voltage and lout is the channel set current), when N=3 and lout=30mA, Vout<3.87V is obtained, and because Vout=VCC-M \* VL-R1 \* lout(M is connected in series on a single channel. When M=8, R1>138 $\Omega$  is obtained. In addition, in order to keep the output constant current, Vout>0.8V is required, so R1<240 $\Omega$ . In order to make the chip have better output characteristics under the condition that the power consumption meets the requirements, it is recommended that R1 choose an appropriate intermediate value.



Package Diagram: SSOP10





Symbol	Dimensions	In Millimeters	Dimension	s In Inches
Symbol	Min	Max	Min	Max
А	-	1.75	-	0.067
A1	0.1	0.225	0.004	0.009
A2	1.30	1.50	0.051	0.059
b	0.39	0.48	0.015	0.019
С	0.21	0.26	0.008	0.01
D	4.70	5.10	0.185	0.201
Е	3.70	4.10	0.146	0.161
E1	5.80	6.20	0.228	0.244
е	1.0	(BSC)	0.039	(BSC)
L	1.05	(BSC)	0.041	(BSC)
θ	0 °	<b>8</b> °	0 °	<b>8</b> °

All specs and applications shown above subject to change without prior notice

(The above circuits and specifications are for reference only. If the company makes corrections, it will not be notified.)