Characteristic description

With the high performance and reliable quality, TM1925 is the nine-channel LED constant current driver control dedicated circuit, integrated with circuits such as MCU single-wire digital interface, data latch, LED constant current driver and PWM brightness control internally. As chip can be cascaded through the single-wire digital interface (DI, DO), peripheral control unit can control the chip and follow-up chip cascaded with it only with a single wire. The PWM brightness at TM1925 output port can also be set separately through peripheral control unit. VDD pin is internally integrated with a 5 V Zener diode with few peripheral devices. The product has excellent performance and reliable quality.

Functional characteristics

- CMOS technology is provided
- The OUT output port can withstand 24 V voltage
- 5 V Zener diode is internally integrated in VDD, of which can support 6~24 V voltage after concatenating a resistance
- The brightness regulation circuit can adjust 256 grades of brightness
- Single-wire serial cascade interface
- Vibration mode: RC vibration is integrated internally. Clock synchronization can be realized according to signals on data cable. Follow-up data can be automatically regenerated and transmitted to subordinate through data output terminal after receiving data of this unit. Signals don't distort or attenuate with cascade being further
- Power-on reset circuit is integrated internally
- Internal control mode (colorful flicker)
- PWM control terminal can realize 256 grades of regulation, with a scanning frequency of 7 KHz.
- The reception and decoding of data can be completed through a signal line
- At the refresh rate of 30 fps, cascade number is no less than 1024 bit and data transmission rate can be up to 800 Kbps
- Transmission distance between any two points is no less than 30 m
- Package type: SOP14, DIP14

Internal structure diagram

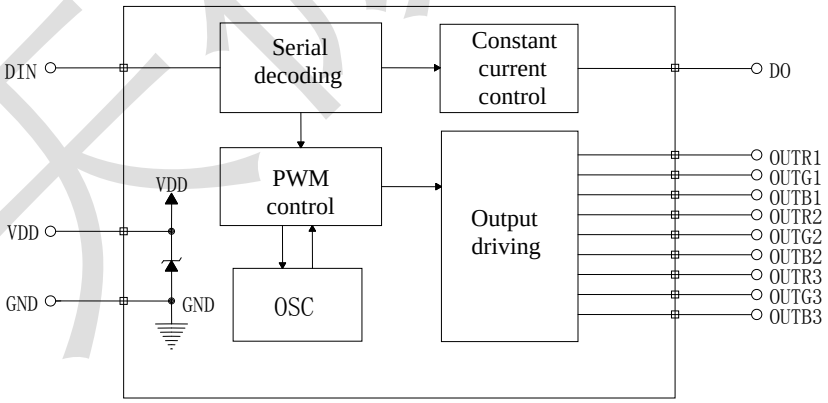


Diagram 1

Pin configuration

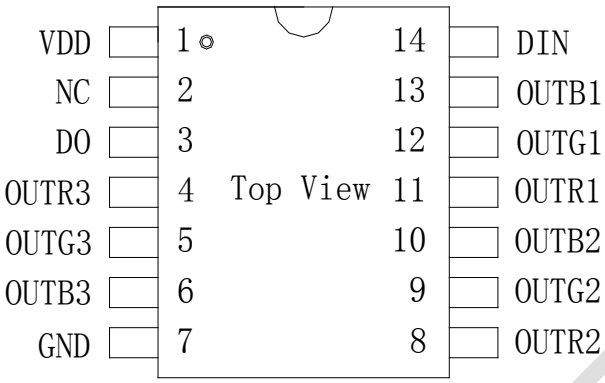


Diagram 2

Pin function

Port		I/O	Function Description
Name	Pin		
DIN	14	I	Data input
DO	3	O	Data output
NC	2	-	Empty pin
OUTB1	13	O	Blue PWM constant current output
OUTG1	12	O	Green PWM constant current output
OUTR1	11	O	Red PWM constant current output
OUTB2	10	O	Blue PWM constant current output
OUTG2	9	O	Green PWM constant current output
OUTR2	8	O	Red PWM constant current output
OUTR3	4	O	Red PWM constant current output
OUTG3	5	O	Green PWM constant current output
OUTB3	6	O	Blue PWM constant current output
VDD	1	-	Logic power
GND	7	-	Grounded system

Equivalent circuit of output and input

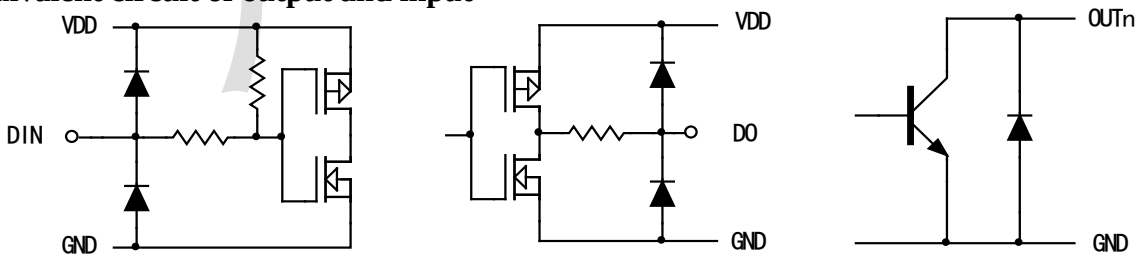


Diagram 3

Integrated circuit is SSD, which is easy to produce mass static in dry season or dry environment. As electrostatic charge may damage the integrated circuit, Titan Micro Electronics suggests taking all appropriate preventive measures for protecting integrated circuit. Improper operation and weld may damage the ESD or degrade its performance to make the chip unable to work normally.

Limit parameters (1) (2)

Parameters			Scope	Unit
VDD	Voltage of logic power		-0.4～+7.0	V
Vin	Voltage scope of input terminal	DIN	-0.4～VDD+0.7V	V
Iout	Current of output terminal (DC)	OUTR, OUTG, OUTB	19～21	mA
Vout	Voltage scope of output terminal	OUTR, OUTG, OUTB	-0.4～+30.0	V
Fosc	Rate of DIN clock	DIN	400～900	KHz
Topr	Scope of Operating temperature		-40～+85	℃
Tstg	Scope of Storage temperature		-55～+150	℃
ESD	Human body mode (HBM)		3000	V
	Machine mode (MM)		200	V

(1) As operating chip at the grades in above table for long time may cause permanent damage to devices and lower the reliability of devices, we suggest never operating chip beyond these limit parameters under any other conditions;

(2) All voltage values are tested relatively to system.

Range of recommended operating condition

(Under -40℃~+85℃, GND=0 V) Unless otherwise specified			TM1925			Unit
Parameters		Test condition	Minimum	Typical value	Maximum	
VDD	Power voltage		4.5	5.0	5.5	V
V_{DIN}	Withstanding voltage scope of DIN input	VDD=5 V, DIN cascades with a 1K resistance	-0.5	--	VDD+0.4	V
V_{DO}	Withstanding voltage scope of DO output	VDD=5 V, DIN cascades with a 1K resistance	-0.5	--	VDD+0.4	V
V_{OUT}	Withstanding voltage scope of OUT output	OUT=OFF	-0.5	--	24.0	V
TA	Scope of operating temperature		-40		+85	℃
TJ	Scope of operating junction temperature		-40		+125	℃

Electrical characteristics

(Under VDD=5.0 V and -40℃~+85℃, typical value VDD=5.0 V and TA=+25℃) Unless otherwise specified			TM1925			Unit
Parameters		Test condition	Minimum	Typical value	Maximum	
VOH	Output voltage of high level	IOH=-6 mA：DO	VDD-0.5	VDD	VDD+0.5	V
VOL	Output voltage of low level	IOL=10 mA：DO			0.4	V
VIH	Input voltage of high level	VDD=5.0 V	3.5		VDD	V
VIL	Input voltage of low level	VDD=5.0 V	0		1.35	V
IOH	Output current of high level	VDD=5.0 V, SDO=5.0 V		1		mA
IOL	Output current of low level	VDD=5.0 V, SDO=1.0V		10		mA
Iin	Input current	DIN connect VDD or GND	-1		1	μA
Icco	Current of logic power (VDD)	OUTR,OUTG, OUTB,DIN, DO=open circuit	1.2	3.0	4.2	mA
Iolc	Scope of constant output current	OUTR, OUTG, OUTB= 3.0V	19	20	21	mA
Iolkg	Output leakage current	OUTR, OUTG, OUTB =OFF	0		0.3	μA
Tpwm	Duty ratio of OUT port	OUT connect pull-up resistor	135	140	145	μs
ΔIolco	Constant-current error (Channel to channel)	OUTR, OUTG, OUTB =ON ,VOUTn =1V			±3	%
ΔIolc1	Constant-current error (Chip to chip)	OUTR, OUTG, OUTB =ON , VOUTn =1V			±6	%
ΔIolc2	Line regulation	OUTR, OUTG, OUTB =ON , VOUTn =1V		±0.5	±1	%/V
ΔIolc3	Load regulation	OUTR, OUTG, OUTB =ON , VOUTn =1V～3V		±1	±3	%/V
IDDdyn	Dynamic current loss	OUTR, OUTG, OUTB =OFF DO=Open circuit			3	mA
Rth(j-a)	Thermal resistance value	--	79.2		190	℃/W
PD	Consumed power	(Ta=25℃)			1.15	W

Switch characteristics

(Under VDD=5.0 V and -40℃~+85℃, typical value VDD=5.0 V and TA=+25℃) Unless otherwise specified						
Symbol	Parameters	Test condition	Minimum	Typical value	Maximum	Unit
Fosc	Rate of DIN clock	VDD=5.0V	-	800	-	KHz
FOUT	Output frequency of OUT PWM	OUTR, OUTG, OUTB	6.5	7	7.5	KHz
tPLZ	Propagation delay time	DIN → DOUT			200	ns
tPZL	--	CL = 15pF, RL = 10K Ω			100	ns
TTHZ	Fall time	CL = 300pF， OUTR、OUTG、OUTB			80	μs
CI	Input capacitance	--			15	pF

Time sequence characteristics

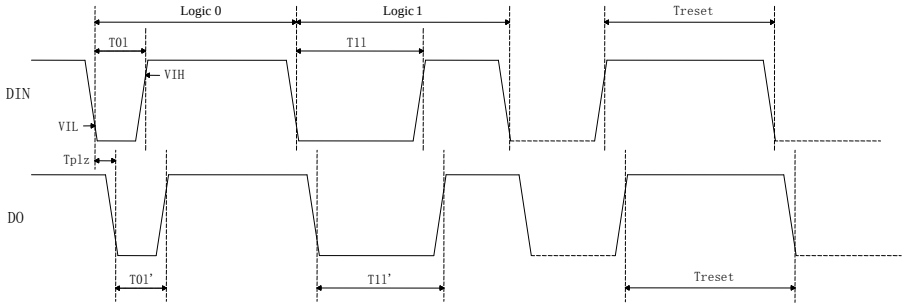


Diagram 4

Function Description

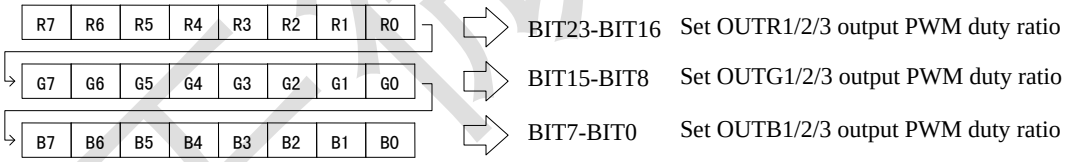
With single-wire communication mode, this chip sends signals in the way of return to one code. After power-on reset, the chip receives 24×3 bit data from DIN terminal, and then DO port starts to forward the data continually sent from DIN terminal to provide input data for next cascade chip. Before forwarding data, DO port is under high level all the time. If DIN inputs RESET signal, the chip will receive 24×3 bit data and output corresponding PWM duty ratio after successful reset, and wait to receive new data again. After completely receiving the beginning 24×3 bit data, data are forwarded through DO port. Before receiving the RESET signal, the original output of OUTR, OUTG and OUTB pins remain unchanged.

As the chip is provided with automatic shaping forwarding technology, signals will not distort or attenuate so that cascade number is only limited by the requirements of screen renewing speed but not signal transmission.

Data structure

PWM mode command:

If this data package is PWM setting data in 24 bit data package. Its structure is shown as follows:



The above is the PWM data format set for the first group of RGB. Setting a piece of TM1925 needs 3 groups of data packages with the same format.

PWM duty ratio is continuously adjustable from 0-256. The 24×3 bit data are transmitted from high to low according to the sequence of RGB. Every 24 bits can be spitted into 3 data of 8 bit to be transmitted. The high level time between bytes shall be no more than the time of RESET signal, otherwise the chip will reset to receive data again, and data transmission cannot be realized.

Communication rate

Symbol	Parameters	Test condition	Minimum	Typical value	Maximum	Unit
T0L	Input 0 code, low level time	VDD=5V GND=0V	150	300	450	ns
T1L	Input 1 code, low level time		600	750	900	ns
T0L’	Input 0 code, low level time		--	340	--	ns
T1L’	Input 1 code, low level time		--	680	--	ns
T	Cycle time of 0 code or 1 code		--	1200	--	ns
Treset	Reset code, high level time		140	500		μs

Note: the cycle time of transmitting 0 code or 1 code is 1200 ns (800 KHz frequency).

Data transmission and forward

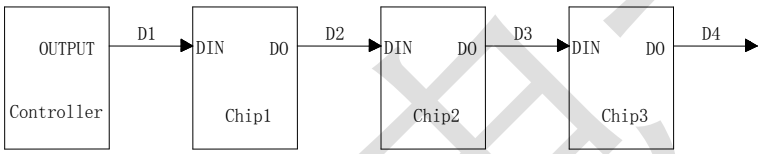


Diagram 5

D1 is data transmitted by controller and D2, D3, D4 are data forwarded by cascade TM1925.

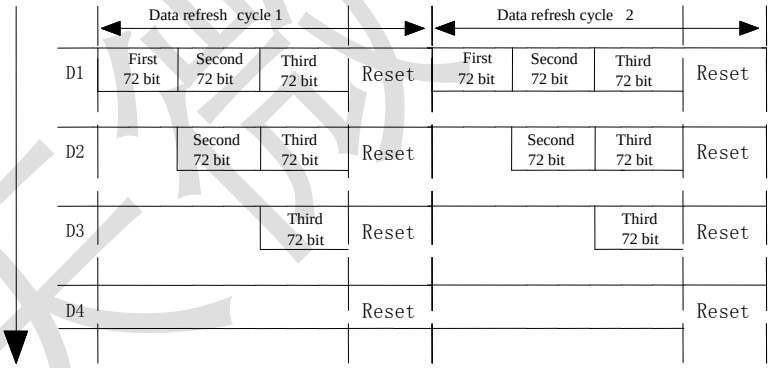


Diagram 6

The process of chip cascade and data transmission and forwarding: Controller sends data (D1); when Chip 1 received the first 72 bit, it doesn’t begin to forward data (D2). Then controller sends data continuously and Chip 1 receives the second 72 bit. Since Chip 1 has stored the First 72 bit, when Chip 1 forwarded the second 72 bit through DO and Chip 2 received data (D2) forwarded from Chip 1, Chip 2 doesn’t begin to forward data (D3). Next, controller sends data continuously and Chip 1 forwards the third 72 bit to Chip 2. Since Chip 2 has stored a 72 bit, it will forward the third 72 bit (D3). After Chip 3 receives the third 72 bit, if controller sends a RESET high level signal at that time, all chips will reset and output the 72 bit data respectively received through three groups of RGB ports to complete a data refreshing cycle. Chips returns to reception readiness.

Internal control mode

When chip power is normal and DIN is tested to be no input signal, or 600 ms after original normal signal missed, chips will enter internal control mode and flicker circularly as follows.
The flicker principle of internal control mode is as follows:

	RGB Status		
Status No.	**R**	**G**	**B**
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1
5	1	0	1
6	0	1	1
7	1	1	1

Remarks: “0” means light off and “1” means light on.

Application information

1. How to calculate data refreshing rate

Data refreshing time is calculated by the number of pixels cascade in a system. Usually, a group of RGB is a pixel (or a section). A TM1925 can control 3 groups of RGB.

Calculation is generally made according to normal mode:

The highest transmission rate of a BIT is 1,200 ns (800 KHz frequency). As a pixel data totally contains 24 Bits including red (8 BIT), green (8BIT), blue (8BIT), the transmission time is 24×1.2 uS=28.8 uS. Hence, if there are 2,000 pixels in a system in all, the time of once refreshing all display will be 28.8 uS×2,000=57.6 mS (neglecting the time of RESET code), i.e. the refresh rate in a second is: 1÷57.6×1,000≈17.36 Hz.

The table of highest data refreshing rate corresponding with cascade points is shown as follows:

	Normal mode	
Pixel	**Time of fastest refreshing data (mS)**	**Highest refreshing rate (Hz)**
1～500	14.4	69
1～800	23.04	44
1～1,000	28.8	35
1～1,500	43.2	23
1～1,800	51.84	19
1～2,000	57.6	17

If data refreshing rate is not required too much for system, there will be no requirement for the number of cascade pixel matrixes. Theoretically, TM1925 infinite cascades can be used only if power supply is in normal condition.

2. How to make TM1925 in best constant current condition

TM1925 output is constant current driver. According to the constant current curve of output, under 20 mA constant current, the voltage of OUT terminal entering into constant current area shall be more than 1.2 V to produce constant current on chip. However, this OUT terminal voltage is not the higher, the better. Since higher voltage leads to larger power consumption on chips, serious chip heating will reduce the reliability of whole system. Therefore, it is suggested to control the voltage Vout within 1.2~3 V when OUT terminal is on. Also, series resistance mode should be used commonly for operation. Theoretical calculation of resistance is shown as follows:

System driving voltage: VDD
Turn-on voltage drop of single LED: Vled
Number of LED in series: n
Constant current value: Iout
Voltage of constant current: 1.5 V
Resistance: R

$$R = (VDD-1.5-n\times Vled)/ Iout$$

For example: If the power supply of the system is 24 V, the turn-on voltage drop of single LED is 2 V, number of LED in series is six and constant current value is 20 mA, it can be calculated according to above formula that: R=(24-1.5-2×6)/0.02=525 Ω, i.e. only a resistance about 525 Ω is required to cascaded on the pin of OUT.

3. How to expand current with TM1952

Each OUT terminal of TM1952 can only output 20 mA constant current at most. For any requirement of driving with larger constant current value, three OUT terminals can be shortly jointed for operation, as each short circuit of OUT can increase 20 mA constant current value and at most 60 mA constant current can be generated after three shortly circuits. The disadvantages of this method are software is required to cooperative with control and 3 register values shall be recorded while advantages are that the required current value can be obtained precisely and constant current is relatively large.

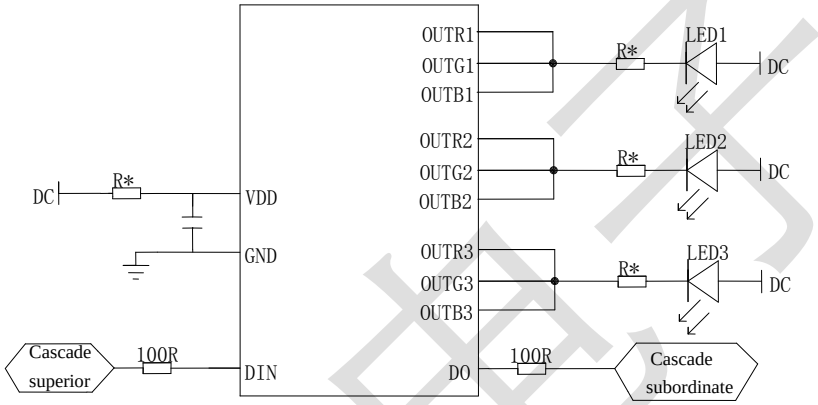


Diagram 7

4. Power configuration

TM1925 can be configured to be 6~24 V voltage to supply power while different power resistances shall be configured according to different voltages. The calculation method of resistance is: since power voltage is reduced with the improvement of load in practical application, current flowing through VDD pin is calculated as 10 mA and therefore the resistance of VDD is R= (DC-5.5 V)/10 mA (DC is power voltage).

List of configured resistance value is shown as follows:

Power voltage DC	Suggested resistance value between power interface and VDD
5V	Resistance is not required and internal Zener diode doesn't work.
6V	50Ω
9V	350Ω
12V	650Ω
24V	1.8KΩ

5. Method of driving LED by program

5.1 Voltage of RGB ports shall be guaranteed to get chips entered into constant current to realize the control of chips to the brightness of LED (Refer to “Constant Current Curve” for details).

5.2 Power on and reset the chips. Port voltage reaches 1.2 V and constant current of RGB of output channel is 20 mA, so the allowable maximum current is 20 mA.

5.3 LED brightness can be adjusted arbitrarily by changing PWM value. If the PWM value is 0, the output will be full and LED will be off. If the PWM value is set to FFH, the output will be maximum low-level duty ratio and LED will be on.

Constant current curve

When apply TM1925 to LED panel design, electricity difference between channels will be very small, which derives from the excellent characteristics of TM1925:

- Besides, the stability of output electricity will not be influenced when load terminal voltage changes, as is shown in Diagram 8.
- Driving current on TM1925 port is constant current value.

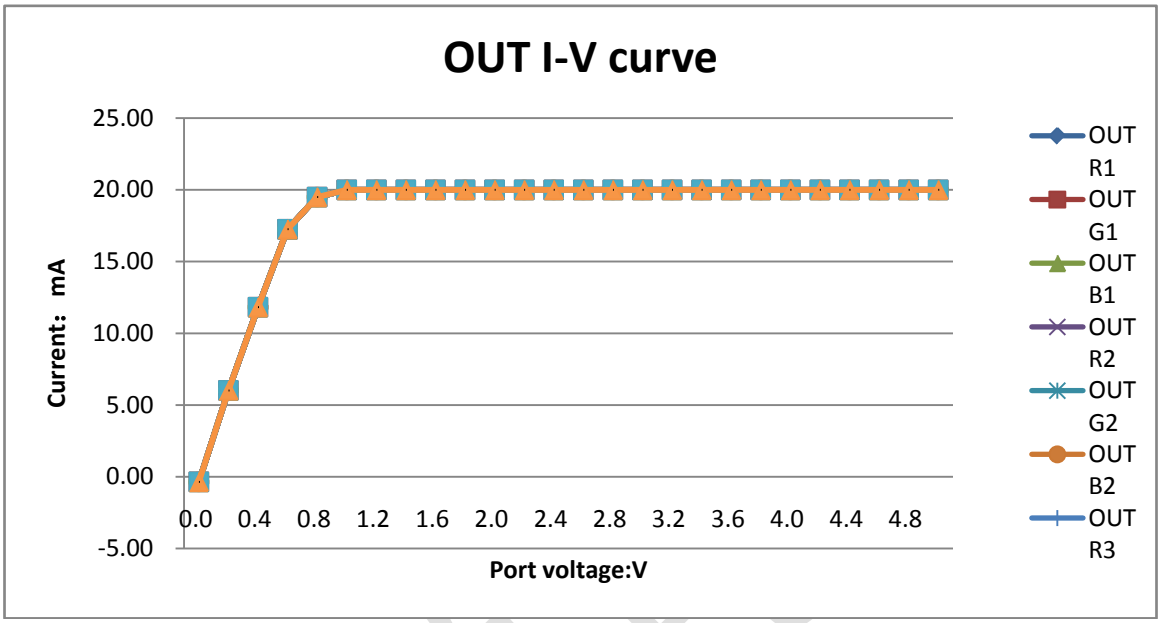
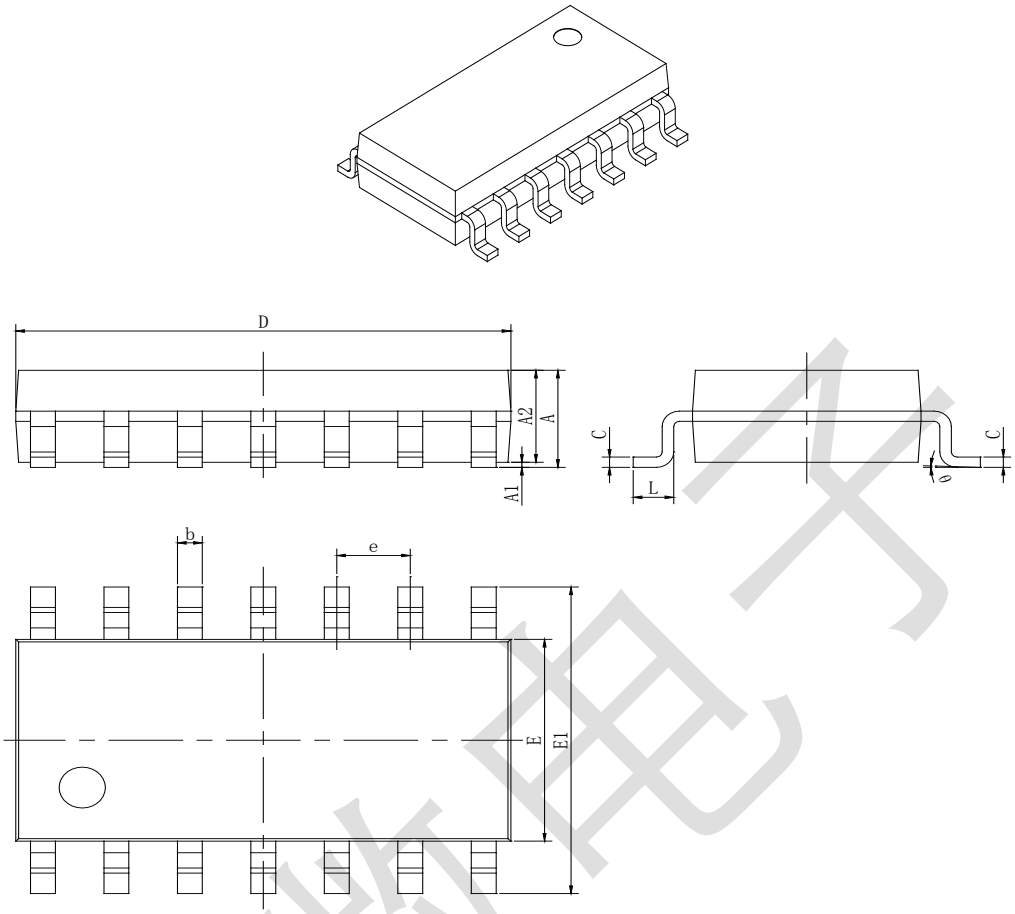


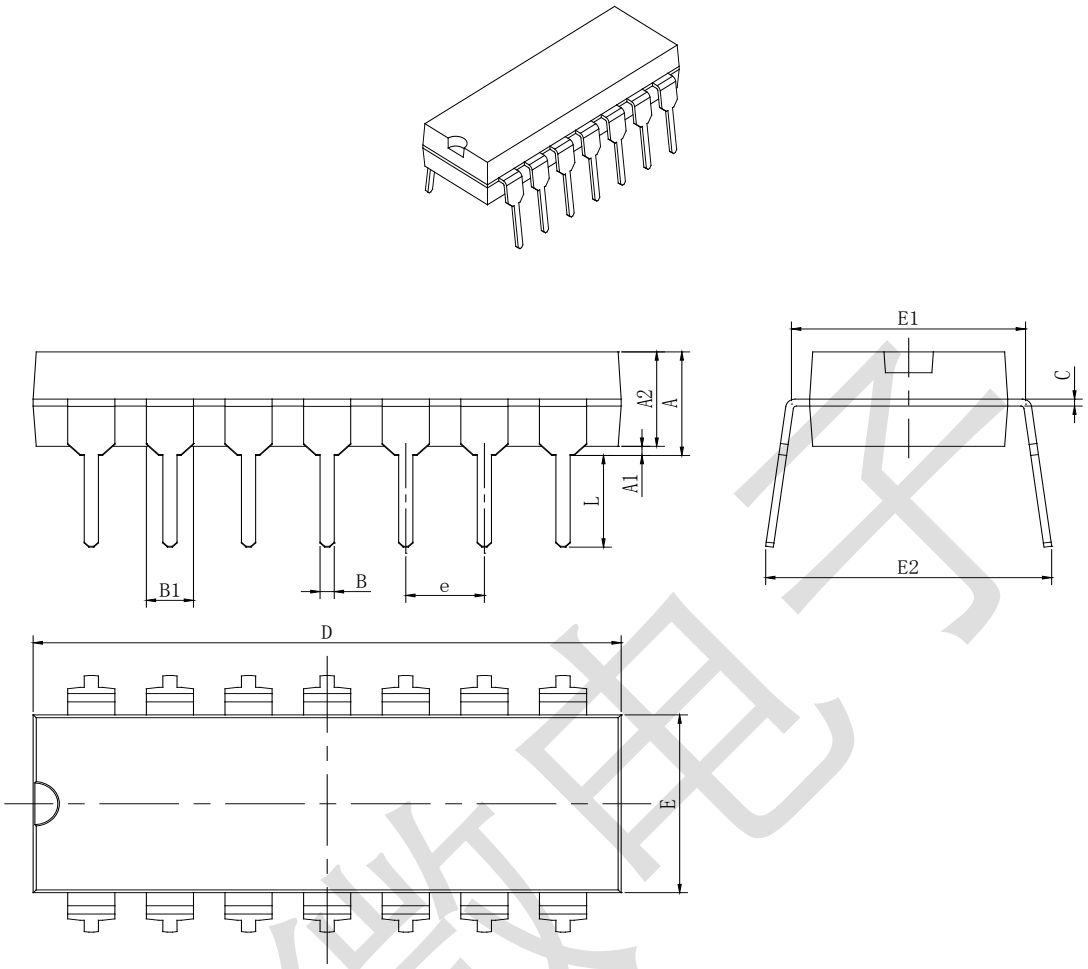
Diagram 8

Packaging diagram (SOP14)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	8.360	8.760	0.329	0.345
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Packaging diagram (DIP14)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524(BSC)		0.060(BSC)	
C	0.204	0.360	0.008	0.014
D	18.800	19.200	0.740	0.756
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540(BSC)		0.100(BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

All specs and applications shown above are subject to change without prior notice.
(Above circuits and specifications are for reference only. Revisions can be made without notice.)